REMARKS

This paper is being filed as a response to the Office Action of June 27, 2008. Reconsideration is respectfully requested in view of these clarifying remarks.

Rejections under 35 USC § 102

Claims 1-6, and 14-20 were rejected under 102(b) as being anticipated by U.S. Patent No. 5,822,599 to Narayan et al. This rejection is respectfully traversed.

The Examiner is reminded that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, the identical invention must be shown in as complete detail as contained in the claim. *Richardson v. Suzuki Motor Co.*868 F.2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim.

The Examiner is also reminded that the claimed invention as a whole must be considered. "[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103." In re Sponnoble, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969).

The Office has failed to analyze Applicant's claims as a whole, instead breaking-down rejections into incoherent pieces that poorly show how the prior art arguably teaches the featured claims. For example, claim 1 defines an input socket configured to receive data packets. The Office has asserted that this feature is anticipated by Narayan because "the input data from I/O module of the system intended to be used." While this statement may be

true, this statement offers absolutely no information on how Narayan anticipates Applicants' claims, and the Office's rejection is improper.

Additionally, claim 1 defines a networking application processor comprising a memory for storing instructions. The Office has asserted that this feature is anticipated by Narayan in "main memory of the Narayan ... system or instruction cache 204, see Fig. 2." Applicants respectfully disagree. The person skilled in the art will readily appreciate that main memory does not reside in a processor. In fact, Fig. 2 of Narayan describing a processor does interface with the memory subsystem, therefore the main memory does not reside in the processor. The Office has chosen to ignore the claim as a whole, and the Office's rejection is improper because main memory does not reside in the processor.

Further, claim 1 defines circuitry configured to access data structures associated with a processing stage, the circuitry configured to access data structures enabling a single cycle access of an operand from a memory location (emphasis added). The Office has not even offered an explanation of how Narayan teaches the circuitry configured to access data structures, and has merely pointed to where Narayan supposedly teaches a memory location. Further yet, the Office has not put forward either an explanation on how Narayan anticipates a single cycle access of an operand in claim 1.

In addition, claim 1 defines circuitry for aligning operands to be processed by the ALU, the circuitry for aligning operands causing the operands to be aligned by a lowest significant bit, wherein the circuitry for aligning the operands supplies an extension to the operands to allow the ALU to process different size operands (emphasis added). Instead of teaching how Narayan teaches this limitation, the Office has instead decided to explain how

Narayan teaches a different limitation, by changing the language of the claim and instead describing how Narayan teaches "causing the operand" (in singular) "to be aligned," and "circuitry for aligning the operand" (in singular). Under a 102 rejection, the Office must state how all of the claim limitations are anticipated by the prior art. Changing the Applicants' claim language is inappropriate and misleading. Even assuming *arguendo* that Narayan taught circuitry of aligning the operand, this does not anticipate circuitry for aligning the operands, as claimed by Applicants. Applicants respectfully request that the Office clearly explains how the potential prior art teaches Applicants claims using the exact language of the claims, or using obviousness arguments to explain the differences.

Claim 14 defines a processor capable of processing a data packet associated with a processing stage of a pipeline of processors. The Office has asserted that Narayan teaches the pipeline of processors because "each pipeline stage does processing and therefore any pipelined processor contains a 'pipeline of processors,'" and pointed to the following excerpt:

> "As used herein, a 'clock cycle' is an interval of time accorded to various stages of an instruction processing pipeline within the microprocessor to complete their various functions. Storage devices (e.g. registers and arrays) capture their values according to a clock signal defining the clock cycle." (col. 1, lines 15-20 - emphasis added).

Applicants respectfully disagree. Narayan teaches an instruction processing pipeline within the microprocessor, which nowhere suggests a pipeline of processors. Suggesting that any pipelined processor contains a pipeline of processors is conclusory and unsubstantiated. The Office is offering a twisted play on words, which any reasonable person skilled in the art would consider inappropriate. Not everything in a system that performs a function is a processor. For example, memory performs a function of storing data, yet a person skilled in the art would never call a memory a processor. The Office has failed to show how Narayan

teaches a processor capable of processing a data packet associated with a processing stage of a pipeline of processors, and the Office's rejection is improper.

Further, claim 14 defines a processor comprising a data random access memory (RAM) configured to enable access to data structures. The Office has asserted that this featured is taught by Narayan "as the main memory." Applicants respectfully disagree. As previously described with respect to claim 1, main memory is not located in the processor, and the Office's rejection is improper.

Additionally, claim 14 defines instruction fetch and decode circuitry configured to interpret instructions to be executed by an arithmetic logic unit, which according to the Office is taught by Narayan in 'early decode units 207A-207D and MROM and anything else related to decoding" (emphasis added). Applicants respectfully disagree. Applicants request that the Office clearly explain how the prior art teaches the claimed limitations. The assertion "and anything else" is overly broad and vague. Applicants respectfully request that the Office points out where each of the specific limitations recited in the rejected claims is found in the prior art relied on in the rejection without mischaracterizing the references. See MPEP, "the examiner should set forth in the Office action ...(A) the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate" (MPEP 706.02(j)-emphasis added).

Further, claim 14 defines that the instruction fetch and decode circuitry includes a read only memory (ROM), the ROM configured to store code common to each processing stage associated with a pipeline of processors. The Office has asserted that the ROM is anticipated by Narayan in "portion of the MROM" (emphasis added). Applicants

respectfully disagree. The Office has once more used vague language such as "portion" that fails to explain how the prior art teaches Applicants' claims. Moreover, Narayan teaches that "MROM unit 209 parses and serializes the instruction into a subset of defined fast path instructions to effectuate a desired operation" (col. 6, lines 29-31). Thus, a MROM does not suggest a ROM, although the names sound similar, because MROM unit parses and serializes instructions, and a Read Only Memory stores bits and does not parse and serialize instructions. Thus, Narayan does not teach that the instruction fetch and decode circuitry includes a read only memory (ROM), the ROM configured to store code common to each processing stage associated with a pipeline of processors.

Dependent claim 2 defines the feature wherein the single cycle access enables the data to be addressed and operated on in a single clock cycle without being placed into a register (emphasis added). The Office has asserted that this feature is taught by Narayan in col. 10, last paragraph (excerpted below). Applicants respectfully disagree.

> "During certain clock cycles, instructions may not be fetched by fetch control unit 266. Instead, the valid instructions within instruction bytes fetched during a previous clock cycle may not have been completely transferred to storage devices 254, as indicated by instruction group control unit 260. As used herein, the term "valid instruction" refers to an instruction within the fetched instruction bytes which is intended to be dispatched to decode units 208" (col. 10, last paragraph - emphasis added).

Additionally, the Examiner has asserted the following:

> "Note that if an instruction is fetched, the data contained within that instruction is addressed (with a program counter) and operated on (read from memory). The definition of the word "operate" according to The American Heritage® Dictionary of the English Language, Fourth Edition is to 'perform a function: work'. Under this definition, a read (fetch) from memory is reasonably considered to be an operation" (page 6, second paragraph - emphasis added).

The Examiner has not only ignored considering the claim as a whole, but it seems like the Examiner is trying to redefine the very basics of computer science as understood by the

person skilled in the art. First, the excerpt cited by the Examiner nowhere suggests that the data to be addressed and operated on in a single clock cycle (emphasis added). Applicants respectfully request that if the Examiner maintains this rejection, the Examiner explains where Narayan teaches that the operation is performed in a single clock cycle, so Applicants can clearly explain in the Appeal Brief how Narayan does not teach this feature.

Additionally, claim 2 is referring to accessing data structures because claim 1 defines access[ing] data structures (emphasis added). The Examiner equates an instruction with data because the "data [is] contained within that instruction." The Examiner is playing with the meaning of the word "data" and ignoring that Applicants are claiming "data structures." Thus, fetching instructions does not teach accessing data structures because an instruction is not the same as a data structure, and the Examiner's rejection is improper. Still yet, the Examiner's assertion that reading an instruction from memory is the same as executing an instruction is conclusory and completely ignorant of the basic principles of operation of a processor system. For all these reasons, Applicants assert that Narayan does not anticipate that the single cycle access enables the data to be addressed and operated on in a single clock cycle without being placed into a register, as claimed by Applicants.

Rejections under 35 USC § 103(a)

Claims 7-13 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Narayan et al. This rejection is respectfully traversed.

Claim 7 is believed to be patentable for at least the same reasons with respect to claim 1 described hereinabove. Additionally, claim 7 includes the features of circuitry configured to access data structures associated with a processing stage, the circuitry configured to access data structures enabling a single cycle access from a memory location. As mentioned above, Narayan is incapable of enabling a single cycle access. The Examiner has provided no basis

for this rejection besides an overly broad interpretation of the claim language by disregarding the specification. In addition the Examiner asserts that the feature of an arithmetic logic unit (ALU), the ALU configured to receive a first and a second operand; the second operand being specified from an internal register, the first operand having a mask enabling the ALU to process a non-masked segment of the first operand. The Applicants respectfully disagree with this characterization as the REGF cited by the Examiner is external to the functional units, i.e., the ALU.

Claim 8 further defines the single cycle access and is patentable over Narayan for at least the above stated reasons with reference to claim 2.

The dependent claims are submitted to be patentable for at least the same reasons the independent claims are believed to be patentable. The Applicants therefore respectfully request reconsideration and allowance of the pending claims. A Notice of Allowance is respectfully requested.

If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 774-6920. **The Commissioner is authorized to charge Deposit Account No. 50-0805 (Order No. ADAPP223), in the amount of $120.00, for a one month extension.** If any other fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. ADAPP223).

Respectfully submitted,
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